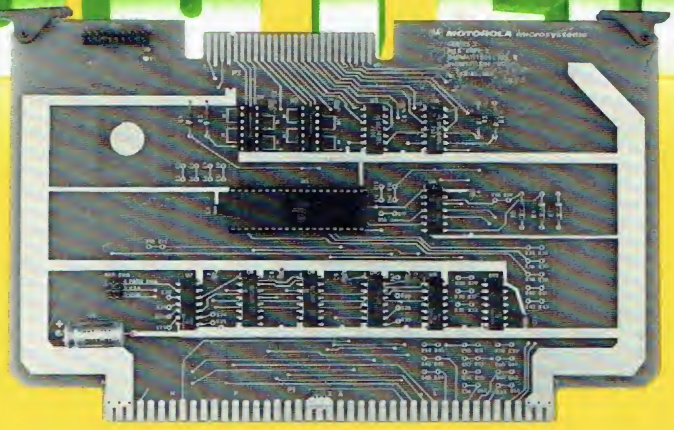
MOTOROLA

MEX68PI2(D)

MEX68PI2
PRINTER INTERFACE MODULE

User's Guide

SYSTEMS



MICROSYSTEMS

MEX68PI2(D)
JULY 1978

MEX68PI2

PRINTER INTERFACE MODULE

USER'S GUIDE

First Edition

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CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides general information, preparation for use, and theory of operation for the MEX68PI2 Printer Interface Module. A typical module is illustrated in Figure 1-1.

1.2 FEATURES

The features of the Printer Interface Module include:

- Provides interface between Motorola 700 Series Printers and the Development System.
- Wire-wrap sockets provided for user custom circuitry.
- Jumper selectable memory map assignment.
- Series II DSB (Dynamic System Bus) provides Page Enable for multi-paged memory and Priority Interrupt patching.
- Bus drive capability.

1.3 SPECIFICATIONS

Printer Interface specifications are identified in Table 1-1.

1.4 GENERAL DESCRIPTION

The MEX68PI2 Printer Interface Module provides the interface between the 700 Series Printers and the Development System. The user can, through custom circuitry, adapt this module as an interface for other printers. Wire-wrap sockets and plated-through holes are provided for this purpose.

The module uses an MC68B21 Peripheral Interface Adapter (PIA) to interface the System MPU to the printer through two 8-bit bi-directional peripheral data buses and four control lines. The address is preset to EC10 for use by the MDOS and EXbug software. The MPU addresses the PIA as though it were memory.

TABLE 1-1. Printer Interface Module Specifications

CHARACTERISTIC	
Interface Type	MC68B21 PIA (2 MHz)
Input Signals	TTL voltage compatible
Data Bus	Three-state TTL voltage compatible
Operating Temperature	0^{o} to 70^{o} C
Power Requirements	+5 Vdc (1.0 A max.)
Dimensions	
Width and Height	9.75 inches x 6.15 inches
Board Thickness	0.062 inches

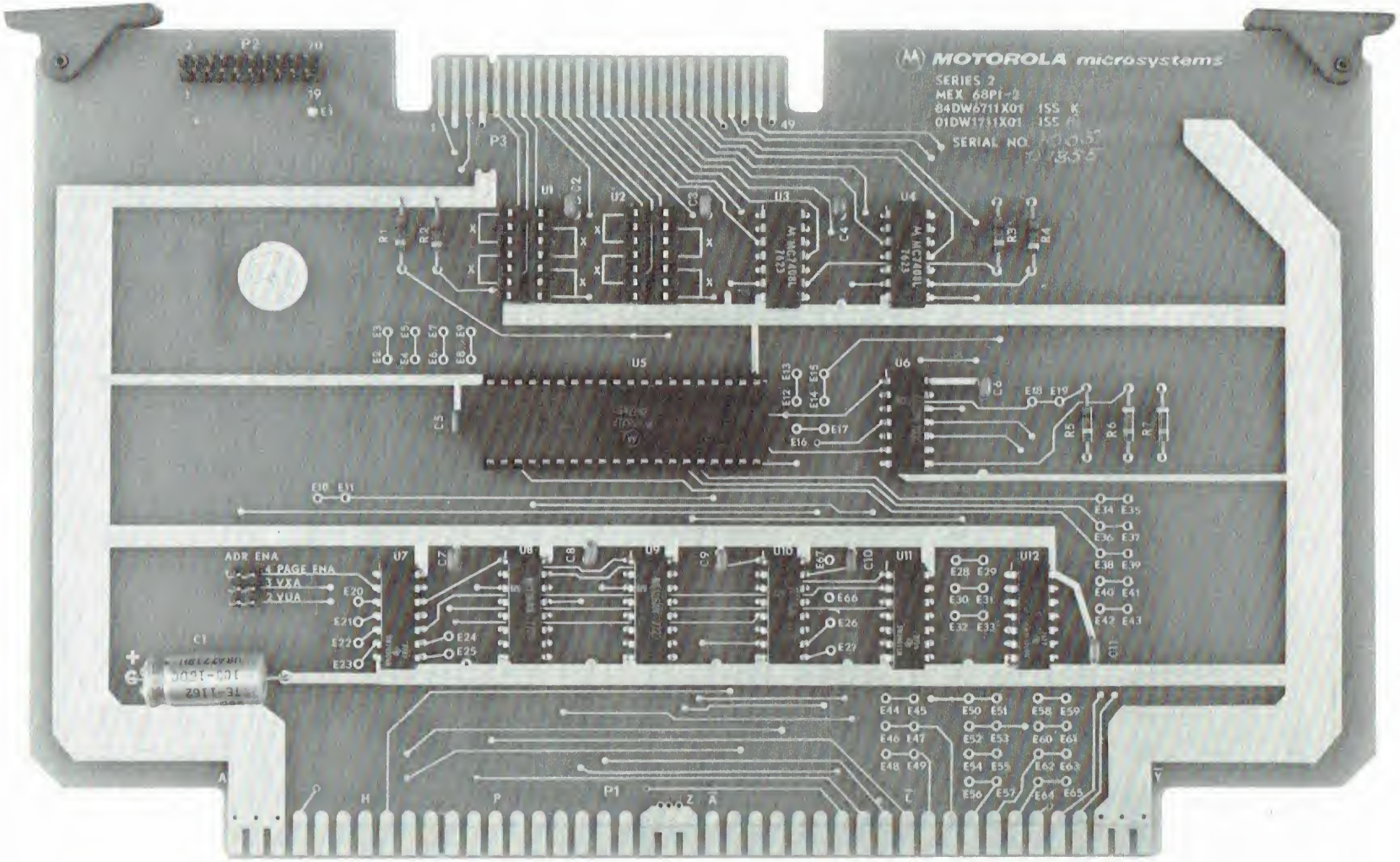


FIGURE 1-1. Typical Printer Interface Module

CHAPTER 2

INSTALLATION INSTRUCTIONS, HARDWARE PREPARATION, AND INTERCONNECTION CONSIDERATIONS

2.1 INTRODUCTION

This chapter provides the unpacking, inspection, installation, and preparation for use instructions for the MEX68PI2 Printer Interface Module. Also included in this chapter are the module interconnection signals.

2.2 UNPACKING

Unpack the MEX68PI2 Printer Interface Module and the MEX68PIC Printer Interconnect Cable from the shipping carton. Refer to the packing list and verify that all of the items are present. Save the packing materials for storing and reshipping the items. If the shipping carton is received in a damaged condition, request that the carrier's agent be present while the module is being unpacked and inspected.

2.3 INSPECTION

The Printer Interface Module and the Interconnect Cable should be inspected upon receipt for broken, damaged or missing parts, and physical damage to the printed circuit board.

2.4 HARDWARE PREPARATION

The Printer Interface Module is populated with a Peripheral Interface Adapter, chip select logic, an address enable memory map jumper, and two sockets for user custom circuitry.

2.4.1 Memory Map Assignment

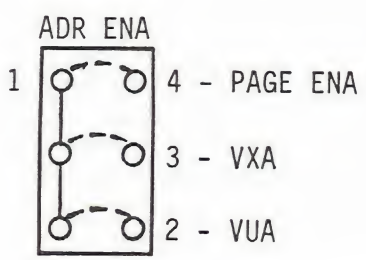
The user must assign the module to one of three map modes. Since the printer is normally used with MDOS and EXbug, the selection is usually VUA for single map mode or VXA for dual map mode.

VUA - Valid User Address

VXA - Valid Executive Address

PAGE ENABLE - For multiple "pages" of 64K bytes

A jumper at ADR ENA is used for this purpose, as illustrated below:



2.4.2 Dynamic System Bus (DSB)

The DSB header P2 offers the users the interconnect capability for PAGE ENABLE (P2-19) and an $\overline{IRQ}$ interrupt at E1 which could be connected to the DSB.

2.4.3 Address "Don't Care" Option

The circuit track connecting the address lines to the chip select logic may be cut as a "don't care" option. To disable a line, cut between the terminal numbers as indicated in Table 2-1.

TABLE 2-1. "Don't Care" Option

ADDRESS LINE	TERMINALS
A0	E34 - E35
A1	E36 - E37
A2	E38 - E39
A3	E40 - E41
A4	E52 - E53
A5	E42 - E43
A6	E64 - E65
A7	E60 - E61
A8	E58 - E59
A9	E62 - E63
A10	E56 - E57
A11	E54 - E55
A12	E50 - E51
A13	E46 - E47
A14	E48 - E49
A15	E44 - E45

2.4.4 Custom Circuitry Considerations

The Printer Interface Module has two 14-pin DIP sockets (U1,U2) for user implementation of special I/O circuitry. The module is factory wired so that each PB line from the PIA is connected directly to connector P3. Each line may be programmed as an input or an output. User supplied devices may be installed in sockets U1 and/or U2. When installing devices in U1 and/or U2, the circuit track must be cut at the points marked "X" on the module.

When the PB lines of the PIA are programmed as inputs, 7402 NOR gates may be used as receivers in U1, U2. When the lines are programmed as outputs, Table 2-2 shows the types of drivers available. Table 2-3 lists the signal description of the MC68B21 PIA device. For further information, see the data sheet for the MC68B21 device.

TABLE 2-2. Driver Types

TYPE	OUTPUT CHARACTERISTIC	INVERTING
7400	TTL	Yes
7401	TTL Open Collector	Yes
7408	TTL	No
7409	TTL Open Collector	No
7426	15V TTL Open Collector	Yes
7437	TTL Buffer	Yes
7438	TTL Buffer, Open Collector	Yes

TABLE 2-3. MC68B21 PIA Interface

PIA PIN	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
10	PB0	PERIPHERAL DATA LINE (PB0) - This peripheral data line in section B of the PIA can be programmed to act either as an input line or as an output line. A "0" in B0 of the B data direction register causes this line to function as an input line; a "1" causes the line to function as an output line. This line has three-state capability allowing it to enter a high impedance state when this line is used as an input.
11	PB1	PERIPHERAL DATA LINE (PB1) - Same as PB0 on pin 10 except bit B1 of the B data direction register controls this line.
12	PB2	PERIPHERAL DATA LINE (PB2) - Same as PB0 on pin 10 except bit B2 of the B data direction register controls this line.
13	PB3	PERIPHERAL DATA LINE (PB3) - Same as PB0 on pin 10 except bit B3 of the B data direction register controls this line.
14	PB4	PERIPHERAL DATA LINE (PB4) - Same as PB0 on pin 10 except bit B4 of the B data direction register controls this line.
15	PB5	PERIPHERAL DATA LINE (PB5) - Same as PB0 on pin 10 except bit B5 of the B data direction register controls this line.
16	PB6	PERIPHERAL DATA LINE (PB6) - Same as PB0 on pin 10 except bit B6 of the B data direction register controls this line.
17	PB7	PERIPHERAL DATA LINE (PB7) - Same as PB0 on pin 10 except bit B7 of the B data direction register controls this line.

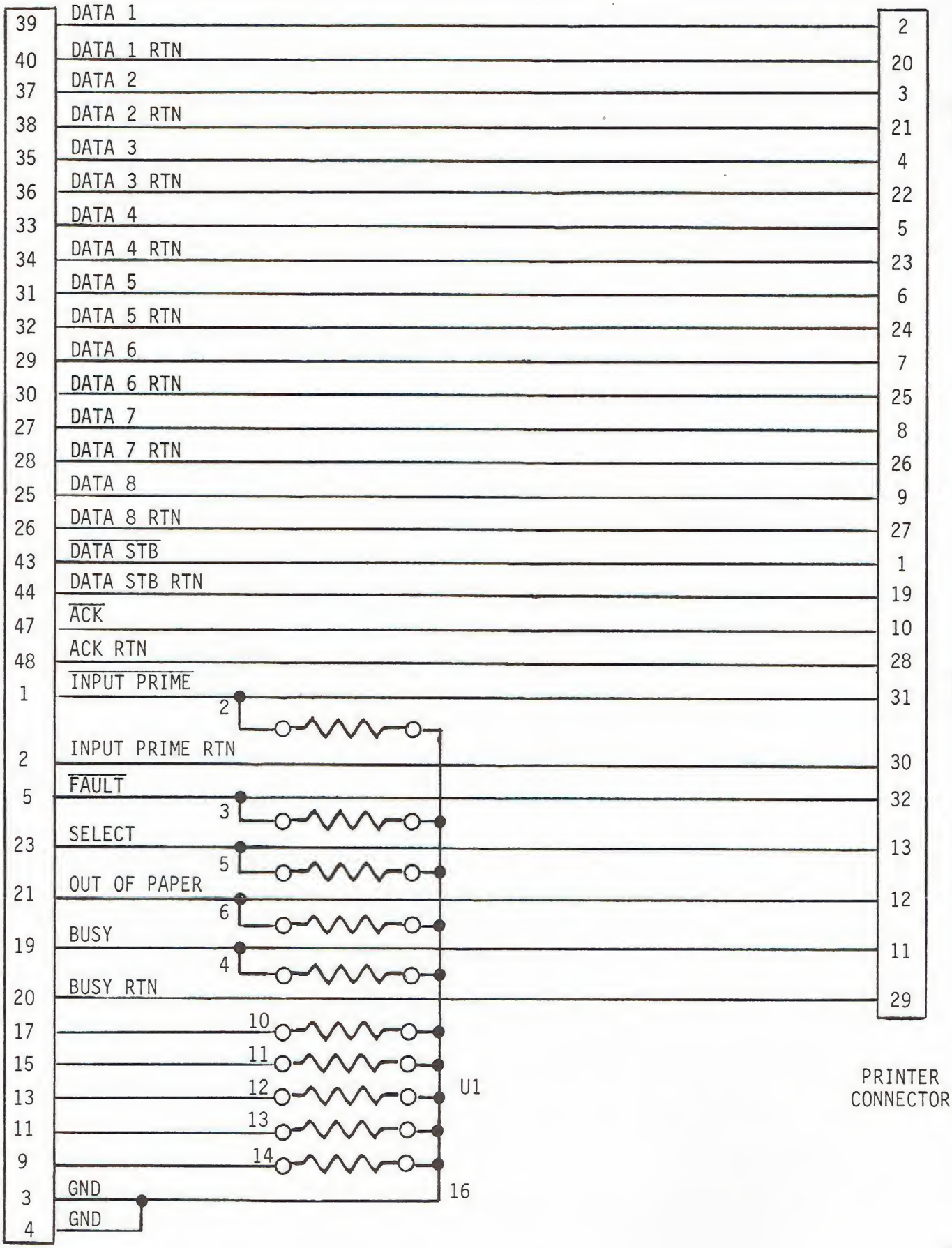


FIGURE 2-1. Interconnect Cable Wiring Diagram

2.5 INTERCONNECT CABLE

The MEX68PIC Printer Interconnect Cable is supplied with the Printer Interface Module. The red line on the flat ribbon cable is aligned with pin 1 on the connector, which mates with P3 on the module. The other end of the cable terminates in a printed wiring board assembly, which serves as a transition between the Printer Interface Module 50-pin connector and the 36-pin printer connector. Figure 2-1 is the wiring diagram of the cable, as supplied. If the user adds custom circuitry to the module or if a printer other than the 700 Series is used, it may be necessary to alter this cable or fabricate a new one.

2.6 INSTALLATION INSTRUCTIONS

Install the Printer Interface Module as follows:

a. Turn the power OFF.

CAUTION

INSERTING THE PRINTER INTERFACE MODULE WHILE POWER IS APPLIED MAY RESULT IN DAMAGE TO THE COMPONENTS ON THE MODULE.

b. Install the module in the selected card slots. This module may be installed in any of the 14 card slots.

c. Install MEXPIC cable supplied and connect to P3 on module. The red line on the ribbon cable must be aligned with Pin 1 on P3.

d. Connect the other end of the interface cable to the printer.

e. Turn power ON.

2.7 MODULE INTERCONNECTIONS

The Printer Interface Module interconnects directly with the system bus. The module bus (P1) signals are identified in Table 2-4. Table 2-5 identifies the interface signals at connector P3.

TABLE 2-4. Connector P1 Bus Interface Signals

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
A, B, C	+5 VDC	+5 Vdc used for the module logic circuits.
D	$\overline{IRQ}$	INTERRUPT REQUEST ($\overline{IRQ}$) - This signal requests than an MPU interrupt sequence be generated within the machine. The MPU will wait until it completes the current instruction that it is executing before it recognizes the request. At that time, if the interrupt mask bit in the MPU condition code register is not set (interrupt masked), the MPU will begin the interrupt sequence. The PIA on the Printer Interface Module, at the user's option, is capable of generating an IRQ signal. Jumper selectable.

TABLE 2-4. Connector P1 Bus Interface Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
E, F, H		Not Used.
J	ø2	Phase 2 (ø2) clock signal.
K - Y		Not Used.
$\overline{A}$ - $\overline{F}$		Not Used.
$\overline{H}$	$\overline{D3}$	DATA BUS ($\overline{D3}$) - This bi-directional line, when enabled, provides a two-way transfer between the MPU Module and the Printer Interface Module. The data bus receivers on this module are continually enabled to receive data. The data bus drivers on this module are in their off or high-impedance state except the module is selected during a memory read operation.
$\overline{J}$	$\overline{D7}$	DATA BUS ($\overline{D7}$) - Same as $\overline{D3}$ on P1-$\overline{H}$.
$\overline{K}$	$\overline{D2}$	DATA BUS ($\overline{D2}$) - Same as $\overline{D3}$ on P1-$\overline{H}$.
$\overline{L}$	$\overline{D6}$	DATA BUS ($\overline{D6}$) - Same as $\overline{D3}$ on P1-$\overline{H}$.
$\overline{M}$	A14	ADDRESS BUS (A14) - This address line, when enabled, transfers the MPU program counter output to the Printer Interface Module
$\overline{N}$	A13	ADDRESS BUS (A13) - Same as A14 on P1-$\overline{M}$
$\overline{P}$	A10	ADDRESS BUS (A10) - Same as A14 on P1-$\overline{M}$.
$\overline{R}$	A9	ADDRESS BUS (A9) - Same as A14 on P1-$\overline{M}$.
$\overline{S}$	A6	ADDRESS BUS (A6) - Same as A14 on P1-$\overline{M}$.
$\overline{T}$	A5	ADDRESS BUS (A5) - Same as A14 on P1-$\overline{M}$.
$\overline{U}$	A2	ADDRESS BUS (A2) - Same as A14 on P1-$\overline{M}$.
$\overline{V}$	A1	ADDRESS BUS (A1) - Same as A14 on P1-$\overline{M}$.
$\overline{W}$, $\overline{X}$, $\overline{Y}$	GND	GROUND
1, 2, 3	+5 VDC	+5 Vdc used for the module logic circuits.
4		Not Used.
5	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ - This signal is used to start the MC68B00 MPU and reset the system from a power down condition or when the system RESTART switch is actuated. This signal resets and initializes the MC68B00 PIA.
6	R/W	READ/WRITE - This MPU output signal indicates to the Printer Interface Module whether the MC68B00 is performing a memory read (high) or write (low) operation. The normal standby state of this signal is read (high). Also, when the MPU is halted, this signal will be in the read state.
7, 8, 9		Not Used.
10	VUA	VALID USER'S ADDRESS - This signal, when high, indicates that the address on the address bus is valid and the system is not addressing the EXbug program. Jumper selectable.
11 - 18		Not Used.

TABLE 2-4. Connector P1 Bus Interface Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
19	VXA	VALID EXECUTIVE ADDRESS - A high-level signal generated by the DEbug Module in place of the VUA signal (refer to description of VUA on Pin 10) when the system is operating in the Dual Map Mode and the EXbug Program is addressing the Executive portion of the memory map. Additionally, all peripheral modules (such as memories) must be set to respond to the VXA signal if the user wants to operate those modules in the Executive portion of the map. Jumper selectable.
29	$\overline{D1}$	DATA BUS ($\overline{D1}$) - Same as $\overline{D3}$ on P1-$\overline{H}$.
30	$\overline{D5}$	DATA BUS ($\overline{D5}$) - Same as $\overline{D3}$ on P1-$\overline{H}$.
31	$\overline{D0}$	DATA BUS ($\overline{D0}$) - Same as $\overline{D3}$ on P1-$\overline{H}$.
32	$\overline{D4}$	DATA BUS ($\overline{D4}$) - Same as $\overline{D3}$ on P1-$\overline{H}$.
33	A15	ADDRESS BUS (A15) - Same as A14 on P1-$\overline{M}$.
34	A12	ADDRESS BUS (A12) - Same as A14 on P1-$\overline{M}$.
35	A11	ADDRESS BUS (A11) - Same as A14 on P1-$\overline{M}$.
36	A8	ADDRESS BUS (A8) - Same as A14 on P1-$\overline{M}$.
37	A7	ADDRESS BUS (A7) - Same as A14 on P1-$\overline{M}$.
38	A4	ADDRESS BUS (A4) - Same as A14 on P1-$\overline{M}$.
40	A0	ADDRESS BUS (A0) - Same as A14 on P1-$\overline{M}$.
41,42,43	GND	GROUND

TABLE 2-5. Connector P3 Interface Signals

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
1	$\overline{INPUT}$	INPUT PRIME - A low-level output signal which clears the printer buffer and initializes the logic. (Not used by all printers)
3	GND	GROUND - Printer Interface Module ground.
5	$\overline{FAULT}$	FAULT - A low-level input signal that indicates a printer fault condition such as paper empty, light detect, or a deselect condition. (Not used by all printers)
7	GND	GROUND - Same as pin 3.
9	PB7	PERIPHERAL DATA LINE (PB7) - See Figure 2-1 and Table 2-3.
11	PB6	PERIPHERAL DATA LINE (PB6) - Same as pin 9.
13	PB5	PERIPHERAL DATA LINE (PB5) - Same as pin 9.
15	PB4	PERIPHERAL DATA LINE (PB4) - Same as pin 9.
17	PB3	PERIPHERAL DATA LINE (PB3) - Same as pin 9.

TABLE 2-5. Connector P3 Interface Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
19	BUSY	BUSY - An input signal indicating that the printer cannot receive data.
21	OUT-PP	OUT OF PAPER - A high-level input indicating the printer is out of paper.
23	SEL	SELECT - A high-level input signal indicating that the printer is selected.
25	PD8	PERIPHERAL DATA LINE (PD8) - Output data to printer from PA7 of PIA.
27	PD7	PERIPHERAL DATA LINE (PD7) - Same as pin 25 except bit A6.
29	PD6	PERIPHERAL DATA LINE (PD6) - Same as pin 25 except bit A5.
31	PD5	PERIPHERAL DATA LINE (PD5) - Same as pin 25 except bit A4.
33	PD4	PERIPHERAL DATA LINE (PD4) - Same as pin 25 except bit A3.
35	PD3	PERIPHERAL DATA LINE (PD3) - Same as pin 25 except bit A2.
37	PD2	PERIPHERAL DATA LINE (PD2) - Same as pin 25 except bit A1.
39	PD1	PERIPHERAL DATA LINE (PD1) - Same as pin 25 except bit A0.
41	GND	GROUND - Same as pin 3.
43	$\overline{\text{DATA STB}}$	DATA STROBE - A 1.0 µsec output pulse used to clock data from the MPU to the printer logic.
45	GND	GROUND - Same as pin 3.
47	$\overline{\text{ACKNLG}}$	ACKNOWLEDGE - A low-level input pulse indicating the input of a character into memory or the end of a functional operation.
49	GND	GROUND - Same as pin 3.
EVEN NUMBERS 2 - 50	GND	GROUND - Same as pin 3.

CHAPTER 3

THEORY OF OPERATION

3.1 INTRODUCTION

This chapter provides a block diagram description of the MEX68PI2 Printer Interface Module (Figure 3-1) and a schematic diagram (Figure 3-2).

3.2 BLOCK DIAGRAM DESCRIPTION

The Printer Interface Module (see Figure 3-1) receives 16 address bits, A0 through A15, along with the ø2 timing signal, the VUA, VXA, or PAGE ENABLE, and the R/W (Read/Write) command during each MPU memory operation. During a memory write operation, this module also receives data bits $\overline{D0}$ through $\overline{D7}$. The module applies address bits A3 through A15 directly to the chip select logic, and address bits A0, A1, and A2 directly to the PIA. VUA, VXA, or PAGE ENABLE is, jumper selectable, applied to the chip select logic.

The control bus interface, after buffering its inputs, applies the R/W command with its complement to the control logic, and the R/W command along with the ø2 timing signal to the control logic and to the PIA.

The control bus interface also receives a $\overline{\text{RESET}}$ command from the system bus when power is first applied to the system, and each time the system RESTART switch is actuated. The $\overline{\text{RESET}}$ signal, after being buffered by the control bus interface, resets and initializes the PIA.

The data bus interface provides a two-way data transfer between the PIA and the system bus. The drivers and receivers in the data bus interface are three-state logic devices and, in their disabled state, provide a high impedance output. The control logic circuit controls the operation of the data bus interface.

The chip select logic determines when the MPU is addressing the PIA. The chip select, on determining that the MPU is addressing the PIA, couples a $\overline{\text{CS}}$ (Chip Select) signal to the PIA and to the control logic. The $\overline{\text{CS}}$ signal with address bits A0, A1, and A2 are used to address the PIA.

During an MPU memory read operation, the control bus interface receives a high-level R/W command and applies this command to the PIA. This interface circuit also applies the R/W command with its complement to the control logic. This high-level R/W command enables the PIA to transfer a PIA status word, direction register status word, or a data word to the data bus interface. At this time, the control logic applies a DREN (Driver Enable) signal to the data bus interface. This signal enables the data bus interface to transfer data from the PIA to the system bus lines D0 through D7.

During an MPU memory write operation, the control bus interface receives a low-level R/W command, and the data bus interface receives an 8-bit data input from the MPU via the system bus. This input may be a data word, a direction register selection word, or a command word. The control bus interface applies a low-level R/W command to the PIA, and the R/W command with its complement to the

control logic. The control logic now applies a $\overline{\text{RCEN}}$ (Receiver Enable) to the data bus interface, enabling this circuit to transfer data from the system bus to the PIA. The PIA at this time is enabled by the R/W command to accept and process the word on the system bus. Data on the PIA peripheral interface lines PA0 through PA7 is output through the drivers and appears at the module connector P3 as PD (Peripheral Data) 1 through PD8. This data is clocked from the MPU to the printer logic by the $\overline{\text{DATA STB}}$ (Data Strobe) output pulse from the PIA. $\overline{\text{ACKNLG}}$ (Acknowledge) is a low-level signal from the printer indicating that a character has been received by the printer.

The PIA, when enabled, couples interrupt commands from the printer to the MC68B00 MPU. The contents of the PIA control registers determine whether the interrupt is enabled and the transition level of the printer interrupt signals to set the PIA interrupt flags. The two $\overline{\text{IRQ}}$ (Interrupt Request) signals ($\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$) are connected to terminal E1.

For further information on the operation of the PIA device, refer to the MC68B21 PIA Data Sheet.

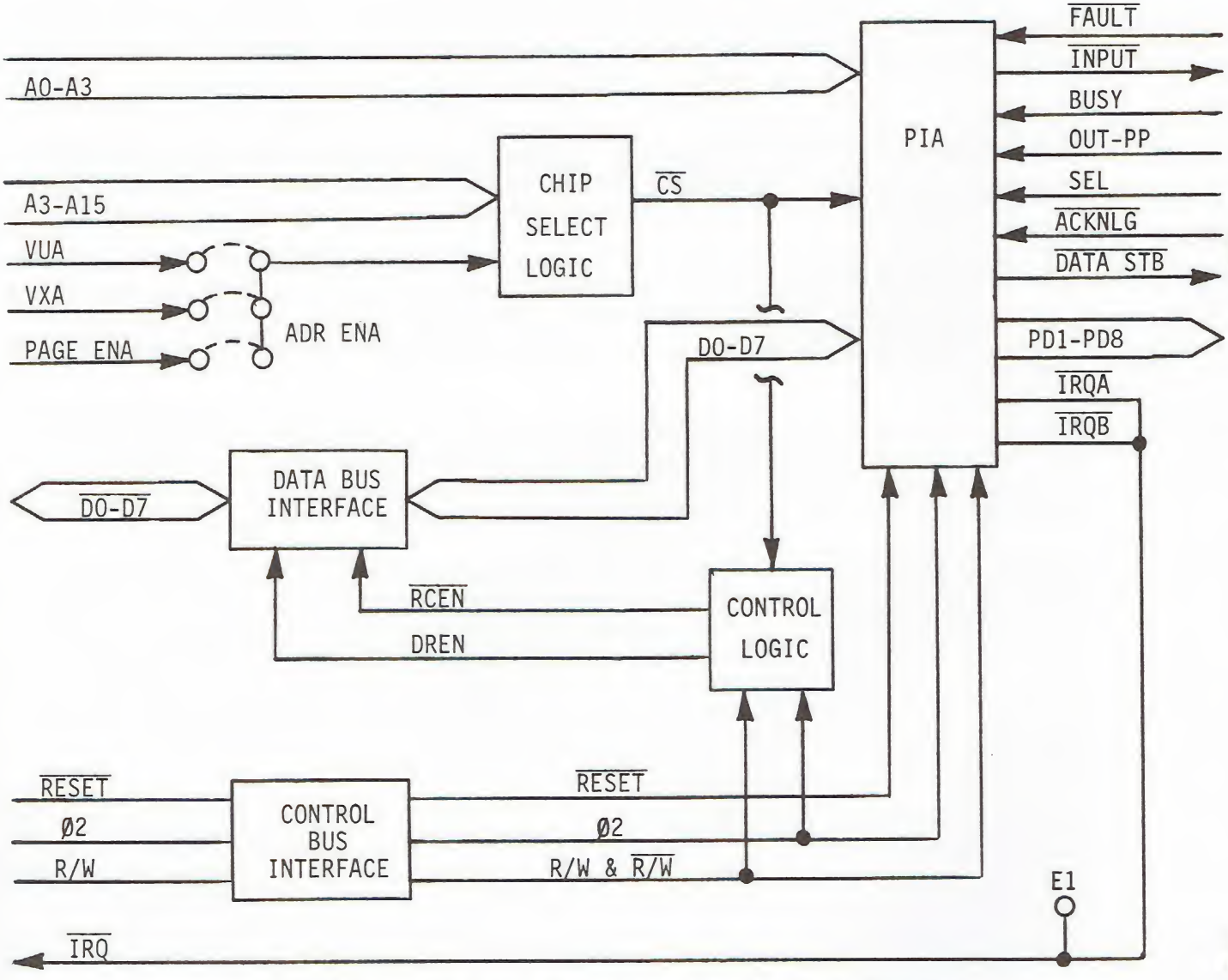
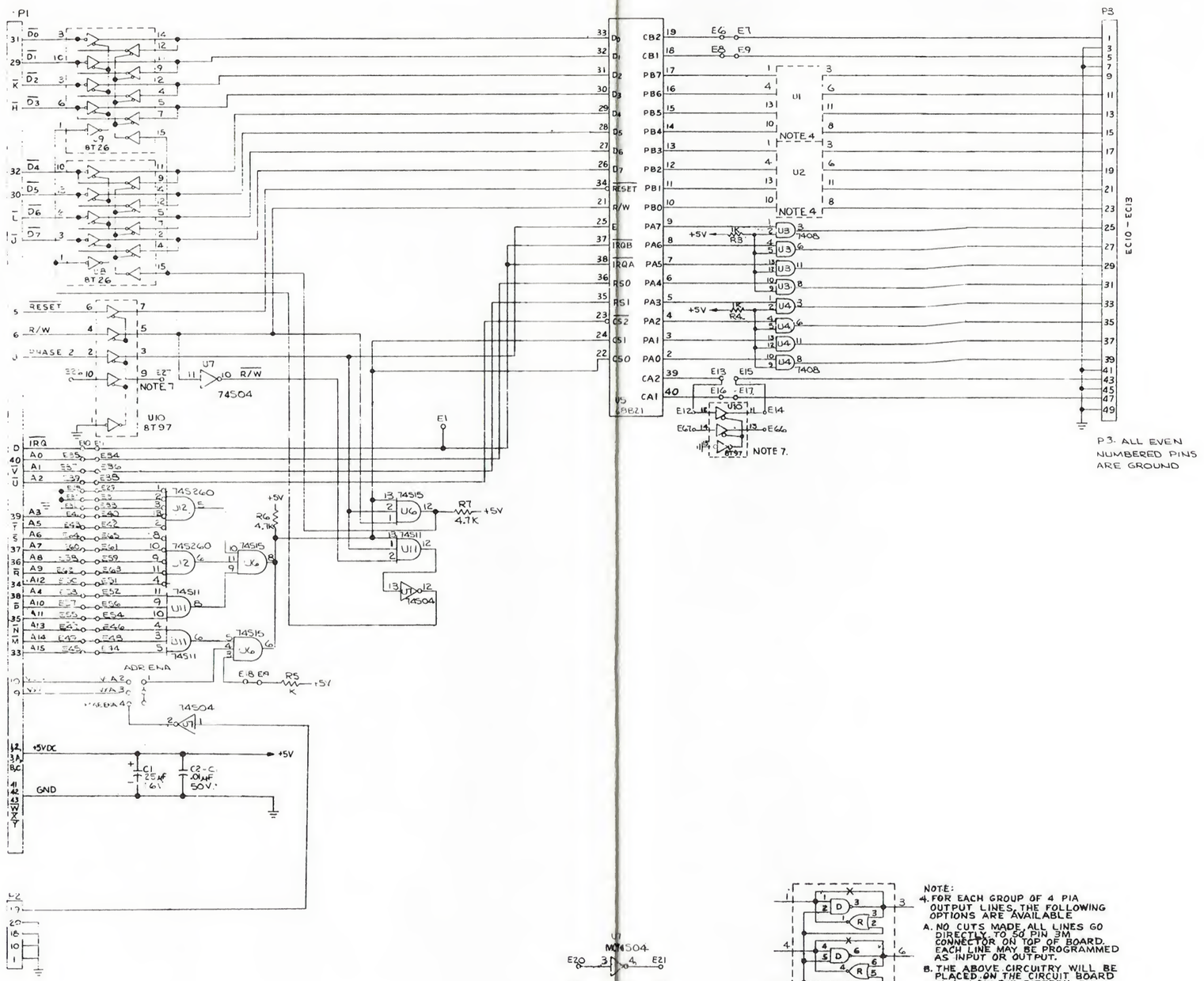


FIGURE 3-1. Printer Interface Module Block Diagram

ECO	ENGR	LET.	CHANGE	BY	DATE
		A	PRO-- , 21 WAS 160 W/R		
B199	[illegible]	K	RELEASE TO PROD.	[illegible]	[illegible]



3. FOR PARTS INFORMATION SEE BM01DW1711X01.
2. MOUNT ALL COMPONENTS ON 84DW6711X01.
1. UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS. CAPACITANCE VALUES ARE IN MICROFARADS.. RESISTORS ARE $\frac{1}{4}$ WATT.

NOTES:

NOTE:
4. FOR EACH GROUP OF 4 PIA OUTPUT LINES, THE FOLLOWING OPTIONS ARE AVAILABLE
A. NO CUTS MADE, ALL LINES GO DIRECTLY TO 50 PIN 3M CONNECTOR ON TOP OF BOARD. EACH LINE MAY BE PROGRAMMED AS INPUT OR OUTPUT.
B. THE ABOVE CIRCUITRY WILL BE PLACED ON THE CIRCUIT BOARD IN A 14 PIN DIP PATTERN. BY CUTTING THE 4 TRACES LABELED X, CUSTOMER SUPPLIED CIRCUITS MAY THEN BE INSTALLED IN THE PATTERN TO SERVE AS EITHER DRIVERS OR RECEIVERS BETWEEN THE PIA OUTPUT AND THE CONNECTOR.
C. WHEN THE 4 LINES ARE PROGRAMMED AS INPUTS, 7402 NOR GATES MAY BE USED AS RECEIVERS.
D. WHEN THE 4 LINES ARE PROGRAMMED AS OUTPUTS, TABLE I SHOWS THE TYPE OF DRIVERS AVAILABLE.

TABLE I - "D" DRIVERS

CKT TYPE	OUTPUT CHARACTERISTIC	INV.
7400	TTL	Y
7401	TTL OPEN COL	Y
7408	TTL	N
~~7409~~	~~TTL OPEN COL~~	~~N~~
7426	15V TTL OPEN COL	
7437	TTL BUFFER	Y
~~7438~~	~~TTL BUFFER, OPEN COL~~	Y

5. IF USING A RECEIVER PACKAGE; CORRESPONDING GROUND JUMPER, E2-[illegible] MUST BE ADDED.
6. IF USING DRIVER PACKAGE; CORRESPONDING PULLUP RESISTOR, R1 AND/OR R2 MUST BE ADDED.
7. TWO NON INVERTING GATES MAY BE USED AS REQUIRED
8. THREE INVERTING GATES MAY BE USED AS REQUIRED

DRAWN BY MJS	DATE 12/21/77
CHECKED BY [illegible]	DATE 1/19/78

TITLE
SCHEMATIC -
PRINTER INTERFACE
MEX-68PI-2 SERIES 2

MOTOROLA INC.
Semiconductor Products Division
[illegible]

DWG NO.
63EW1711X

FIGURE 3-2. Printer Interface Module Schematic Diagram

CHAPTER 4

PARTS

4.1 INTRODUCTION

This chapter provides the parts list and parts location for the Printer Interface Module (Table 4-1 and Figure 4-1), and the parts list for the Interconnection Cable (Table 4-2). The parts list reflects the latest issue of hardware at the time of printing.

TABLE 4-1. Printer Interface Module Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION	EFFEC-TIVITY
	84DW6711X01	Printed Wiring Board, Printer Interface Module.	K
	55NW9403A10	Ejector, Circuit Card, with Roll Pin Attachment, 2 required.	K
C1	23NW9618A33	Capacitor, Electrolytic, 25 MFD at 16 VDC	K
C2-C11	21NW9702A09	Capacitor, Fixed, Ceramic, 0.1 MFD at 50 VDC	L
E1	29NW9805A46	Terminal, Wire-wrap, Feed-Thru, .025 square	K
P2	28NW9802C12	Header, Double Row, Post, 20 Pin	K
R1-R5	06SW-124A49	Resistor, Fixed, Carbon, 1K ohm, 5%, 1/4 W	K
R6-R7	06SW-124A65	Resistor, Fixed, Carbon, 4.7K ohm 5%, 1/4 W	K
U3-U4	51NW9615A37	I.C. MC7408P	K
U5	51NW9615D85	I.C. MC68B21P	K
U6	51NW9615F15	I.C. SN74S15N	K
U7	51NW9615C96	I.C. SN74S04N	K
U8,U9	51NW9615F19	I.C. 8T26A	K
U10	51NW9615B71	I.C. 8T97	K
U11	51NW9615D90	I.C. SN74S11N	K
U12	51NW9615E67	I.C. SN74S260N	K
	28NW9802B09	Socket, DIL, 40 pin (use at U5)	K
	28NW9802B43	Socket, DIL, 14 pin (use at U1, U2)	K
	28NW9802B88	Header, Double Row Post, 6 pin (use at ADR ENA)	K
	29NW9805A91	Jumper, 2 position (use at ADR ENA)	K

TABLE 4-2. Interconnection Cable Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION	EFFEC-TIVITY
U1	84CW6220X01	Printed Wiring Board, Printer Cable	K
U1	51NW9626A11	Resistor Network 15/10K ohm, 16 pin	K
	30NW9302A07	Cable Flat Ribbon, 50 conductor, 28 AWG	K
	28NW9802B32	Connector, Plug, 36 pin	K
	28NW9802A08	Connector, PCB Transfer, 50 pin	K
	28NW9802A56	Connector, PCB Edge Mating, 50 contact	K

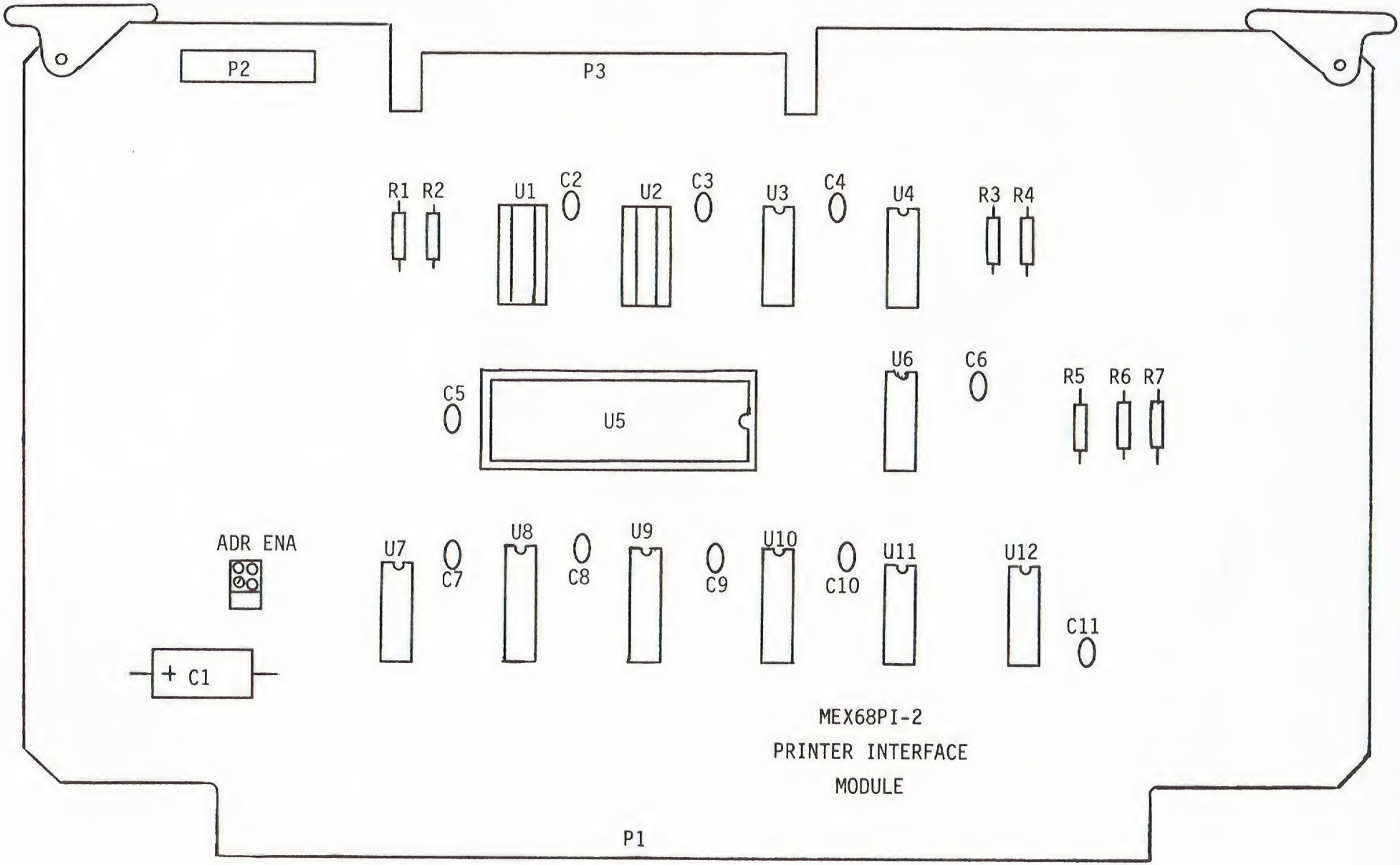


FIGURE 4-1. Printer Interface Module, Parts Location